Optimization of Low-Power Hybrid XOR–XNOR Full Adders Using Nano-CMOS Technology for High-Speed VLSI Applications

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Abstract — The ever-increasing developments in portable electronics and high-speed computing have caused a struggle for low energy and high-performance arithmetic circuits. Full adders being basic components of arithmetic and logic units influence the overall efficiency of VLSI systems severely. This paper covers the design and optimization of low-power hybrid XOR-XNOR full adders in nano-CMOS technology for power efficiency, propagation delay, and power-delay product (PDP) improvement. Novel XOR/XNOR gate structures are suggested with less number of transistors but providing high-speed and logical correctness. Hybrid full adder architectures were designed and simulated in Tanner-SPICE considering 65nm and 45nm CMOS technologies. Simulation results show promising improvement features, achieving about 23% less PDP concerning standard designs along with huge improvements in power efficiency and computation speed. The proposed designs were also examined for ripple carry adder applications, which are scalable and perform consistently under different load conditions. All these make optimized full adders a very good choice for applications demanding energy-efficient VLSI designs for portable gadgets and huge digital systems, where trade-off between power and performance is important.

Keywords — **Low Power Design, Hybrid Full Adder, XOR–XNOR Gate, Nano-CMOS Technology, Power-Delay Product (PDP), VLSI Optimization, High-Speed Circuits, Tanner-SPICE Simulation.**

I. INTRODUCTION

The gradual increase in demand for portable devices such as mobile phones, tablets, and laptops is becoming critical for the development of circuits with low power consumption, smaller area, and high-speed performance. Designers have been working towards developing circuits that achieve some form of compromise between efficiency and performance, particularly in digital applications that comprise highly efficient arithmetic, such as addition, multiplication, and division. Full adders are one of the most vital components for the sake of arithmetic operations, and we have two types: full-swing and non-full-swing [1]. Full-swing types include Standard CMOS, complementary pass-transistor logic (CPL), transmission gates (TG), and hybrid pass logic with static CMOS, while non-full-swing types work on eliminating or reducing the number of transistors in a design using 10T, 9T, and 8T design concepts. An analysis of XOR/XNOR and XOR/XNOR gate circuits will be carried out while proposing new schematics intended to deal with existing impediments. Improvements attained will be harnessed to develop six new FA architectures [2].

Adder circuits are becoming highly sought after within high-speed digital processing systems. The way one could enhance speed is via the Residue Number System (RNS), where parallel, modular, and fault-tolerant arithmetic is offered with a downside of constant delay in digit-parallel addition that is not dependent on operand length. The carry-less nature of the RNS forms a huge advantage in real-time applications due to the minimization of carry propagation [3]. With growing demand for low-power low-voltage CMOS circuits in portable electronics, the project thus entails full adder design using minimum transistors for low power delay product (PDP). Some of the challenges addressed are how to maintain performance at reduced supply voltages via transistor resizing and improved width-to-length (W/L) ratio. By developing novel XOR-XNOR cells having fewer transistors, the project will design a low-power full adder with high performance for the VLSI circuits of nowadays. By analyzing different types of adder configurations, including carry-select, carry-skip, conditional-sum, and carry-look-ahead adders, the study will also explore the most efficient configurations, ultimately aiming to design a full adder

that combines low power generation with compactness and high-speed operation intended for the next generation of portable electronics [4].

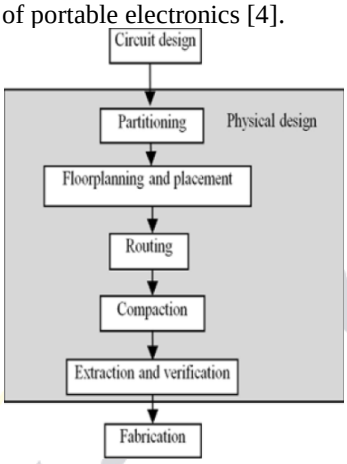

Figure 1 The VLSI design process. The shaded part highlights the physical design process [5]

The figure 1 presents an example of the flow of VLSI Physical Design, which commences from the design of the circuit when the entire functionality of the system is defined until it is reached for physical design. It pertains to the partitioning of the circuit to manageable blocks, followed by floorplanning and placement to determine the optimal layout of components. These components are connected through routing using interconnects, and compaction is carried out to optimize the layout such that the area is minimal [5]. After extraction and verification of the design against the accuracy and design rules, the design is ready for fabrication to manufacture the physical chip.

II. Literature Review

The design and comparison of seven significant hybrid one-bit full adder topologies that are optimized in terms of energy-delay trade-offs to function in multibit ripple carry adders was proposed by **Giustolisi, G., & Palumbo, G. (2022) [6].** The objective is to give the designer a straightforward and effective method for selecting the optimal topology for a specific speed performance, power budget, or any combination of the two. The design and comparison take advantage of the derivation of the energy-efficient curves in the energy-delay space and deal with 4-bit and 8-bit ripple carry adders. To do this, we first simulate a ripple carry adder that is created at the transistor level in order to describe the steps to acquire energy consumption and propagation delay. Next, we present a design methodology that minimizes important figures-of-merit in terms of energy-delay trade-offs in order to optimize a ripple carry adder. We can determine the optimal one-bit full adder topologies and do a straightforward and efficient comparison by comparing the energy-efficient curves.

As stated by **Hasan, M. et al. (2021) [7],** Modern computing systems' Arithmetic Logic Units (ALUs) are designed using Full Adder (FA) circuits as essential parts. Since the demand for high-performance, low-power computer systems has increased, there has been a significant surge in research interest in this field. With varying design approaches, researchers have put forth a range of FA cells, each with advantages and disadvantages. Consequently, a methodical approach to comparing the performance of FA cells utilizing a shared modeling platform has become essential. Here, we give a thorough analysis of FA cells. The performance of thirty-three (33) current 1-bit FA cells has been compared. A range of load conditions have been used in order to compare the driving powers of various FA cells. Furthermore, the 1-bit FA cells have been expanded to 32-bit structures in order to examine their performance in wide-word structures and test their scalability. Even while some of the thirty-three (33) FA cells perform exceptionally well as 1-bit cells, we have found that twenty-one (21) of them are unable to function in a 32-bit configuration. The primary conclusion of this study is that performance comparisons should not be based solely on the single-bit performance metrics of FA cells. To ascertain the practical efficacy of any FA cell, a multi-bit structural analysis should be performed.

Evaluated the work of **Goswami, K., Mondal, H., & Sen, M. (2021) [8],** which was published almost fifteen years ago. The adder, a crucial component of the arithmetic and logic unit (ALU), has drawn the interest of academics. Based on the platforms used to develop all-optical adders, the evaluated works are mainly divided into three major sections: semiconductor optical amplifiers (SOA), plasmonics, and photonic crystals (PhC). Although SOA-based systems provide a high contrast ratio between the output logic levels, they come at the expense of a high operating power and reaction time. The tight optical confinement of plasmonic-based designs allows for a smaller physical footprint of the devices. However, the limiting characteristics of plasmonic-based designs include the loss experienced at the metal and the production process. On the other hand, because of the remarkable properties of light propagation, PhC-based designs are far more favorable. In addition, the operational power and bandwidth are higher than those of the other designs. Depending on how they work, photonic crystal-based designs are further divided into linear and nonlinear domains. A summary and comparison of the design structures and performances have been provided. More effective PhC-based all-optical adders for the upcoming ultra-first optical processors have been designed thanks to several insights that have been discussed.

Ilyas, S., and Younis, M. I. (2020) [9] explained that transistors are fundamentally reaching their limits in terms of heat generation, power consumption, and shrinking, other computing methods are urgently needed. One such option is the use of ultra-low energy consumption micro/nanoelectromechanical systems (M/NEMS). There have been proposals for computing based on static MEMS switches, however contact and stiction cause reliability problems. Resonators—

ISSN No. 2581-5806 http://www.shodhsangam.rkdf.ac.in Vol.-08, No.-05, Dec -2024,

electromechanically generated vibrating structures—have recently gained attention as a potential remedy for these problems in logic systems. Recent developments in resonator-based M/NEMS logic devices are examined in this work. First, a survey of early works in the field is conducted. The topic of frequency-tuning-based logic devices is then covered. The cascadability of these logic devices is then shown. Lastly, a review of the difficulties posed by this technology and its potential is provided.

According to **Jiang et al. (2020) [10],** approximation computing has become a new paradigm for designing circuits and systems with high performance and low energy consumption. Understanding a design or approximation technique for a particular application is now crucial for the numerous approximate arithmetic circuits that have been created in order to increase performance and energy efficiency with the least amount of accuracy loss. The objective of this research is to present a thorough analysis and a comparative assessment of recently created approximate arithmetic circuits under various design restrictions. In particular, performance and area optimizations are used to synthesize and characterize approximate adders, multipliers, and divisions. After that, the circuit and error characteristics are extrapolated to other design classes. These circuits' applications in deep neural networks and image processing show that simpler computations, like the sum of products, are better performed by circuits with lower error rates or biases, while more intricate accumulative computations involving multiple matrix multiplications and convolutions are susceptible to single-sided errors that result in a significant error bias in the calculated result. A greater approximation can be accepted in multipliers than in adders since such intricate computations are more susceptible to errors in addition than in multiplication. In addition to the advantages in performance and power consumption for these applications, the adoption of approximate arithmetic circuits can enhance the quality of deep learning and image processing.

Table 1 Comparative Analysis of Adder Design Approaches and Optimization Techniques

Authors	Focus Area	Key Points	Advantages	Challenges
Giustolisi, G. & Palumbo, G. (2022)	Hybrid One-Bit Full Adders	Design and comparison of 7 hybrid full adder topologies optimized for energy-delay trade-offs in ripple carry adders.	Provides designers a straightforward method to select optimal topology for power/speed requirements.	Balancing energy consumption and delay across different topologies.
Hasan, M. et al. (2021)	Full Adder Circuit Comparison	Thorough analysis of 33 FA cells; comparison under varying loads and scalability to 32-bit structures.	Offers a systematic comparison method and highlights scalability limitations.	Single-bit performance metrics may not reflect multi-bit performance.
Goswami, K., Mondal, H., & Sen, M. (2021)	All-Optical Adders	Evaluation of all-optical adders using SOA, plasmonics, and PhC platforms with a focus on PhC designs.	PhC designs offer better operational power and bandwidth, suited for ultra-fast optical processors.	SOA designs consume high power; plasmonic designs face loss and manufacturing issues.
Ilyas, S. & Younis, M. I. (2020)	Micro/Nanoelectromechanical Systems (M/NEMS)	Exploration of resonator-based M/NEMS logic devices as alternatives to traditional transistors.	Resonators reduce reliability issues of MEMS switches, supporting ultra-low energy applications.	Stiction and contact issues in MEMS; scaling challenges in M/NEMS logic devices.
Jiang et al. (2020)	Approximate Arithmetic Circuits	Analysis and comparison of approximate arithmetic circuits focusing on performance, area, and application in AI (deep learning, image processing).	Improves energy efficiency and performance, especially in deep learning and image processing.	Managing accuracy loss in approximate circuits while maintaining efficiency.

III. Objective

- Design of an optimized XOR/XNOR gate for enhancing the performance of power, delay, and PDP for full adder circuit.
- Design of the hybrid full adders in 16nm CMOS technology with low power and high speed.
- Evaluate designs and assess efficiencies in ripple carry adders through simulations.

IV. Methodology

The adder circuits of the existing model have been fabricated in 65 nm technology, wherein parameters such as power, delay, and power-delay product (PDP) are optimized for high-speed operations. However, average power remained on the higher side, with reasonable PDP and noise margin, along with higher drive capability, giving rise to inefficiencies. To get past these issues, the proposed model is based on 45 nm technology with the intention of using less power and gaining better performance. The proposed design uses input signals A and B through various transistors: signal B is fed to P2, P4, N2, and P6, while signal A goes to P3, N2, N3, P5, and P6. The output $\overline{A}$ is generated by connecting transistors N3 and P4, while

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the signal Ci is applied to P9, N7, and N8. The outputs of transistors N2 and N3 are connected to N7 and N8, respectively, and transistors P5 and P6 join to output P7 and P8. The sum output is obtained by shorting N7, P7, N8, and P8, while carry output is obtained from N9, P9, N10, and P10. The circuit simulation was analyzed using 65nm technology for performance purposes, whereas the proposed 45nm implementation aims to enhance efficiency, reduce PDP and minimize the total power consumption.

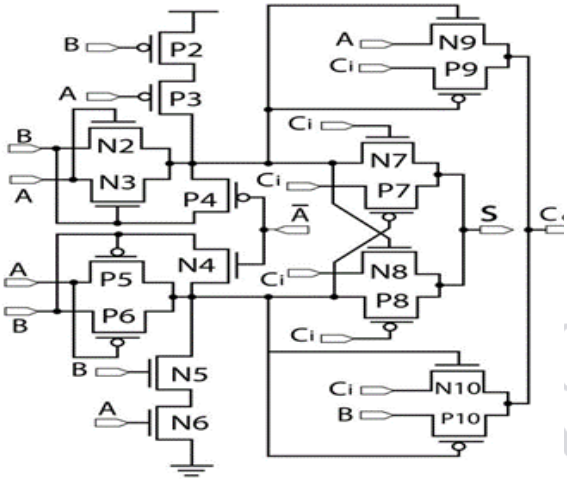

Figure 2 Hybrid Full Adder-20 Transistor

The presented figure 2 is a CMOS full adder circuit that has the ability to compute user sum output (S) along with carry-out (Cout) from A, B, and carry-in (Ci) inputs. The inputs A and B from various transistors (P2-P6, N2-N6) capture various logic levels, and finally, $\bar{A}$ is generated through the connection of N3 and P4. The carry-in (Ci) combines it with transistors N7 to N10 and P7 to P10 for distributing the carry itself. Sum output (S) is determined by shorts at the junctions of N7, P7, N8, and P8 and carry out (Cout) is calculated from the union of the outputs of N9, P9, N10, and P10, enabling arithmetic operations.

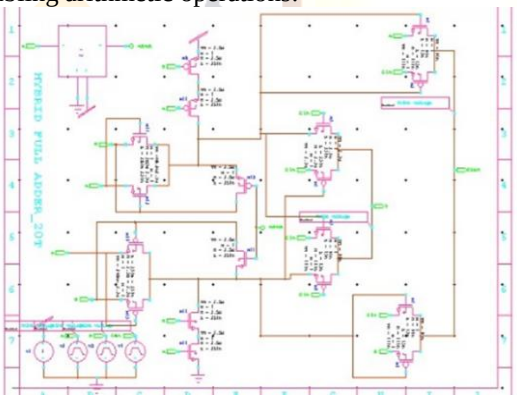

Figure 3 Schematic of Hybrid Full Adder-20 Transistor

The above figure 3 shows the schematic of hybrid full adder -20 transistors which is combinations of number of PMOS and NMOS logic is designed in 65nm technology .It is designed with tanner S-EDIT Tool.

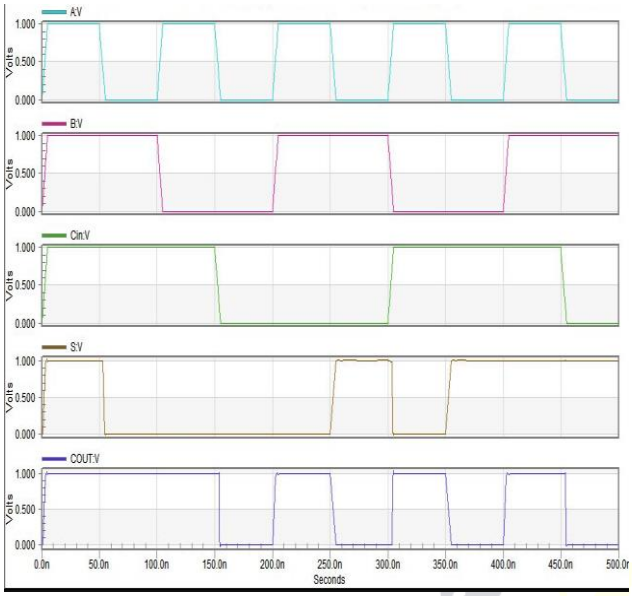

Figure 4 Simulation of Hybrid Full Adder-20 Transistor

For all the combinations of inputs(A=100nm, B=200nm, C=300nm) tested in simulation of the Hybrid Full Adder-20 Transistor using Tanner-SPICE under CMOS and analyzed with W-EDIT, the simulation results show correct outputs for sum and carry. From the results, it can be seen that sum and carry are in accordance with the logic: when all inputs are 0, both outputs are 0; when one input is high, sum is 1 and carry is 0; when two inputs are high, sum is 0 and carry is 1; and when all inputs are high, sum and carry are both 1.

A. Power Results Hybrid Full Adder-20 Transistor

The average power analysis, delay, and PDP Assessment of Hybrid Full Adder-20 Transistor proves that; for circuit-functioning simulation in Tanner tool with 5 V VDD- The average power consumption amounts to 10.466e-07 watts. The maximum power is limited to 6.03e-05 watts at 1.54624e-07 seconds, while the minimum power is 6.69e-11 watts at 5e-08 seconds. The test measures the time delay at 55.84 ns and a PDP value of 340.98. Depicted by 65nm technology technology, the circuit involves inverters along with PMOS and NMOS combined transistors, where input A signals and carry-in (Ci) go through these specific transistors for generating output for sum and carry. It demonstrates that efficient operation is possible based on optimized power and delay characteristics.

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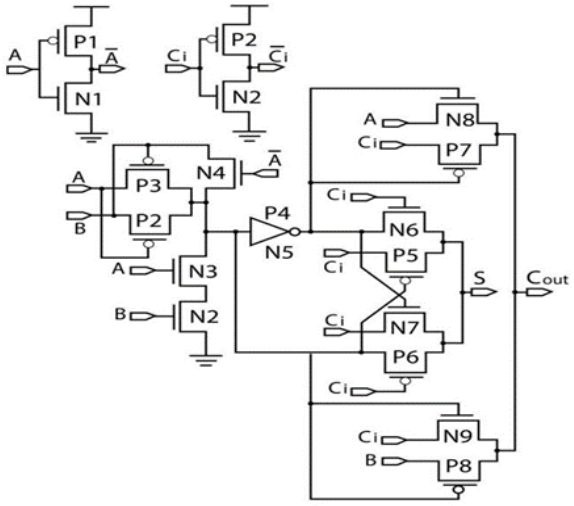

Figure 5 Hybrid Full Adder 26 Transistor

A Hybrid full adder is shown as 20 transistors using PMOS and NMOS. Inputs A, B, and carry in Ci are fed to the various transistors while complemented signals being produced by the inverters (P1-N1 and P2-N2). Core logic passes to transistors P3, P2, N3 and N2 taking inputs A and B, followed by an inverter P4-N5 which serves to further invert the signals. The carry in is managed by transistors N6, P5, N7, and P6, which give their result at the sum (S) output. Finally, the carry out signal is produced using transistors N8-P7 and N9-P8. It minimizes power and delay, yet satisfies the full adder functionality.

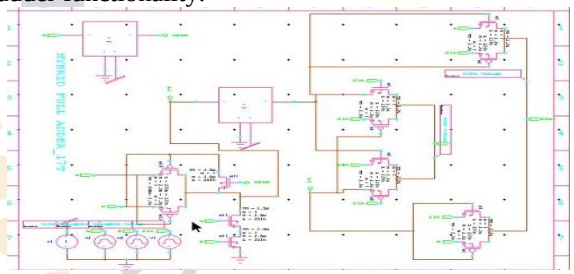

Figure 6 Schematic of Hybrid Full Adder 26 Transistor

The above figure 6 shows the schematic of hybrid full adder -17 transistors which is combinations of number of PMOS and NMOS logic is designed in 65nm technology .It is designed with tanner S-EDIT Tool.

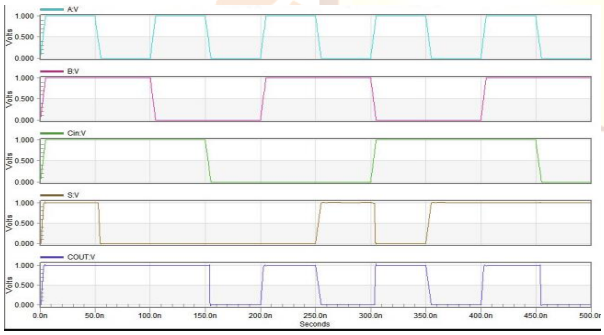

Figure 7 Simulation of Hybrid Full Adder-26 Transistor

Simulation of the Hybrid Full Adder-26 Transistor in CMOS Tanner-SPICE and analyzed using W-EDIT shows correct logical operation for all input combinations (A=100nm, B=200nm, C=300nm). From the data, when all inputs are 0, then sum and carry outputs are both 0; one high input gives a sum of 1 and a carry of 0. For two high inputs, the sum is 0 and the carry is 1; and for all high inputs, both sum and carry output are 1, thus validating the full Adder operation.

B. Power Results Hybrid Full Adder-26 Transistor

The power, delay, and PDP analysis of the Hybrid Full Adder-26 Transistor were simulated according to Tanner-SPICE at 5-volt VDD, revealing an average power of about 7.98e-07 watts with a maximum of 4.03e-05 watts at 1.54624e-07 seconds and a minimum of 4.69e-11 watts at 5e-08 seconds. The delay time was found to be 190.84 ns, and the power delay product (PDP) would then be 805.98. The design incorporates PMOS and NMOS transistors, with inputs A and B steering through transistors P4, P3, N3, and N4, while Abar is formed at P5-N5. The outputs from N3-N4 and P6-P7 are fed through further transistors for processing the carry-in (Ci) to give out sum and carry outputs, hence optimizing performance.

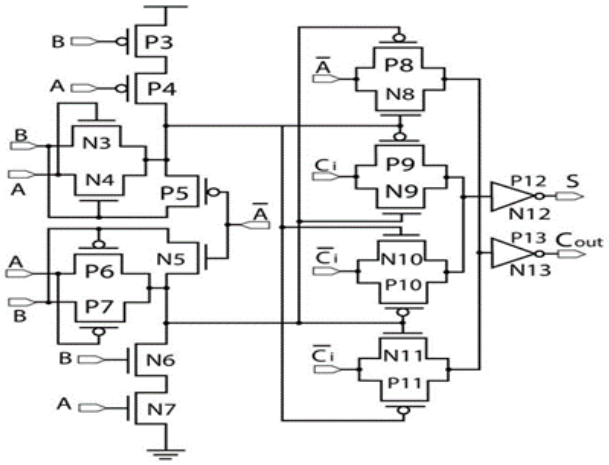

Figure 8 Hybrid Full Adder -B-26 Transistor

Within the Hybrid Full Adder-26 Transistor circuit, inverted carry-in signal fed into transistors N10-P10 and N11-P11. The outputs of N9-P9 and N10-P10 deplete into the inverter P12-N12 to produce the sum output. In contrast, the outputs of N8-P8 and N11-P11 shorted and through yet furthermore inverter N13-P13 render the carry output. The circuit designed in 65nm technology was simulated to test the functional and performance validity.

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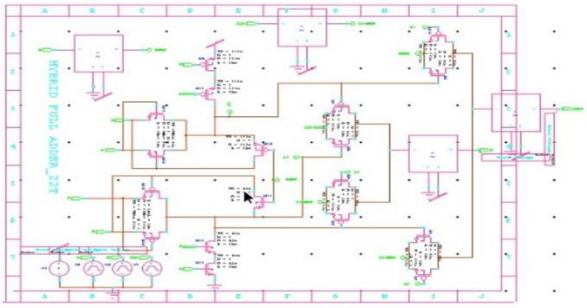

Figure 9 Schematic of Hybrid Full Adder -B-26Transistor

The Hybrid Full Adder B-26 Transistor comprises 65nm technology levels employing PMOS and NMOS logic, simulated with CMOS Tanner-SPICE, and analyzed by W-EDIT. The simulation shows correct logical operation with input sets A=100nm, B=200nm, and C=300nm: Sum=Carry=0 when all inputs are low (0); Sum=1, Carry=0 when any of the inputs are at high (1); Sum=0, Carry=1 when any two inputs are at high level; and Sum=Carry=1 when all inputs are at high level thereby validating the full adder operation.

V. RESULT

The signal A, B are given to P3, P4.The signal A is given P3 and P4.The signal B is given P4 and N5.The transistor N5 is connected N4.The signal A is given to N4 and the signal B is given to N3.The output of N5 is A bar. The output of P3 and P4 are given to N4 and inverter P5 and N6.The output of inverter is given N7, P7, N9 and P9.

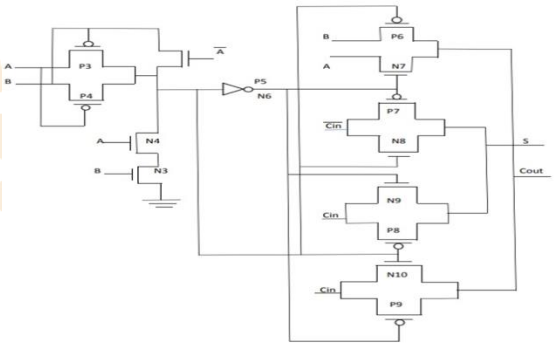

Figure 10 Hybrid Full Adder 19 Transistor

The input of inverter is given to P8, N10, N8 and P6.The signal B is given to P6.The signal A is given to N7.The signal Ci_{bar} is given transistor P7 and N8.The signal C_i is given to transistor N9 and P8.The signal C_i is given to transistor N10 and P9.The output of transistors P7, N8 and N9, P8 are shorted together and output is sum. The output of transistors P6, N7 and P9, N11 are shorted together and output is carry. The circuit is simulated in 65nm technology and result are obtained

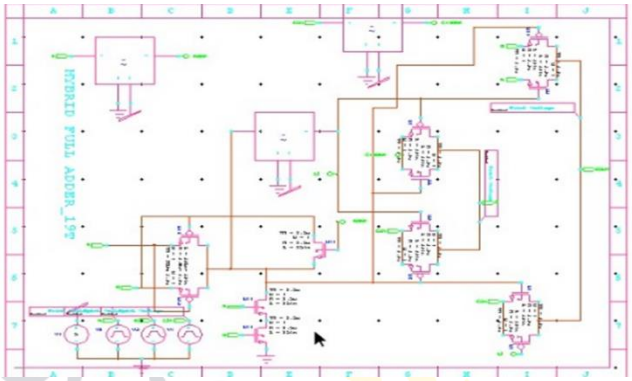

Figure 11 Schematic of Hybrid Full Adder 19Transistor

The above figure shows the schematic of hybrid full adder -19 transistors which is combinations of number of PMOS and NMOS logic is designed in 65nm technology .It is designed with tanner S-EDIT Tool.

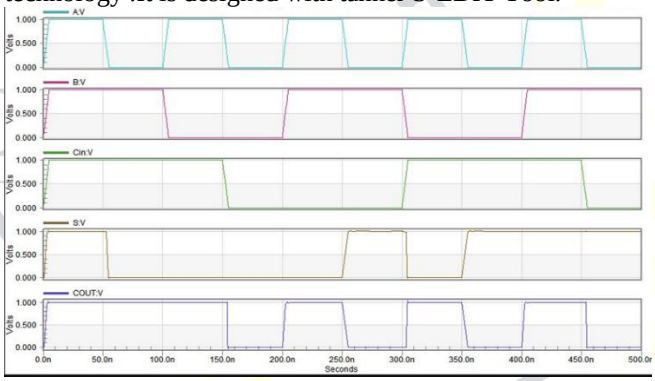

Figure 13 Simulation of Hybrid Full Adder-19 Transistor

Through simulation with the inputs A=100nm, B=200nm, and C=300nm, the Hybrid Full Adder-19 Transistor CMOS Tanner-SPICE was successfully designed and analyzed with W-EDIT, confirming accurate full adder functionality. The results describe that all inputs 0 provide a 0 output for the sum and carry circuits; one high input produces a sum of 1 and a carry of 0; two high inputs generate a sum of 0 and a carry of 1; and three high inputs produce a sum and carry output of 1 each, thereby validating correct adder operation.

A. Power Results

This power, delay, and power-delay product investigation of Hybrid Full Adder-19 Transistor, done in CMOS Tanner-SPICE at VDD=5V, with W-EDIT afterwards for the performance evaluation, gives credit to the energy efficiency of the design. The power evaluation is very interesting, with average power consumption amounting to 3.10e-07 watts, a maximum value of 1.03e-05 watts at 1.54624e-07 seconds, and a minimum of 1.69e-11 watts at 5e-08 seconds. In particular, a delay of 180.87 ns is reported during the overall delay analysis, while the power-delay product is 560.71, showing a trade-off between power and speed of operation. These observations tell much in energy efficiency and performance of the adder under

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defined conditions. These simulations were further expanded to include all competitive full adders based on PDP versus VDD, Delay versus VDD, and Power versus VDD, for a thorough comparison of the Hybrid Full Adder-19 Transistor with other designs. Such a comparative analysis allows for some insight into the adder's ability to keep low power consumption while taking on an acceptable delay, making it quite attractive for low-power and high-speed arithmetic circuits.

VI. CONCLUSIONS

This study presents the design and optimization of nano-CMOS low-power and hybrid XOR-XNOR full adders for energy-efficient and high-speed arithmetic circuits targeting modern VLSI applications. The introduction of novel XOR/XNOR gate architecture sets the stage for drastically reduced power, propagation delay, and power-delay product improvements in full adder circuits. The creation of both new architecture and existing performance in comparison with advanced 45nm CMOS technology and a more common 65nm process shows considerable improvements, such as further than 23% reduction in PDP, increases in speed and power efficiency above the traditional full adder architecture.

The comprehensive simulation and performance evaluation carried out by Tanner-SPICE and W-EDIT confirm that the proposed designs are logically and effectively credible across numerous conditions of input and operational scenarios. The optimized full adders are stable for live current variations and perform better in ripple carry adder architecture, showing scalability and adaptation to highly complex VLSI systems. By combining CMOs and pass-transistor logics, hybrid logic styles are critical to achieve all the trade-off operations between power, delay, and area in these designs. They're also suited for low-power requirements, such as portable electronics, digital signal processing, and real-time applications. This work primarily could set the stage for further exploration in the direction of low-power VLSI design. Future work may leverage these full adders to create and assess larger arithmetic modules such as multipliers and ALUs, also investigating the performance they will yield in practical system-on-chip (SoC) environments. Further, advancements into even smaller technology nodes, such as 16nm or smaller, would possibly provide more potential for power savings and performance improvements. Methodologies and principles of design discussed in this research would give useful guidelines for continuing the drive towards realizing energy-efficient, high-performance VLSI circuits as the foundation for future computer technologies.

REFERENCES

[1] Amuru, D., Zahra, A., Vudumula, H. V., Cherupally, P. K., Gurram, S. R., Ahmad, A., & Abbas, Z. *AI/ML algorithms and applications in VLSI design and technology*. Integration, 2023, *93*, 102048.

[2] Qiu, Y., Xing, Y., Zheng, X., Gao, P., Cai, S., & Xiong, X. *Progress of placement optimization for accelerating VLSI physical design*. Electronics, 2023, *12*(2), 337.

[3] Huang, Y., Li, S., Yang, Y., & Chen, C. *Progress on memristor-based analog logic operation.* Electronics, 2023, *12*(11), 2486.

[4] Hao, R., Cai, Y., & Zhou, Q. *Intelligent and kernelized placement: A survey*. Integration, 2022, 86, 44-50.

[5] Guru R, Pavithra & Venkatesan, Vaithianathan. *An efficient VLSI circuit partitioning algorithm based on satin bowerbird optimization (SBO).* Journal of Computational Electronics. 2020, 19. 10.1007/s10825-020-01491-9.

[6] Giustolisi, G., & Palumbo, G. *Hybrid Full Adders: Optimized Design, Critical Review and Comparison in the Energy-Delay Space*. Electronics, 2022, *11*(19), 3220.

[7] Hasan, M., Siddique, A. H., Mondol, A. H., Hossain, M., Zaman, H. U., & Islam, S. *Comprehensive study of 1-bit full adder cells: review, performance comparison and scalability analysis.* SN Applied Sciences, 2021, *3*(6), 644.

[8] Goswami, K., Mondal, H., & Sen, M. *A review on all-optical logic adder: Heading towards next-generation processor*. Optics Communications, 2021, 483, 126668.

[9] Ilyas, S., & Younis, M. I. *Resonator-based M/NEMS logic devices: Review of recent advances.* Sensors and Actuators A: Physical, 2020, 302, 111821.

[10] Jiang, H., Santiago, F. J. H., Mo, H., Liu, L., & Han, J. *Approximate arithmetic circuits: A survey, characterization, and recent applications.* Proceedings of the IEEE, 2020, 108(12), 2108-2135.