

An architecture for Lifting based 1D-DWT using Canonical Sign Digit

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Abstract: A new architecture namely 2-D DWT, Multiplier-and accumulator (MAC) based Radix-4 Booth Multiplication Algorithm for high-speed arithmetic logics have been proposed and implemented on Xilinx. By combining multiplication with accumulation and devising a hybrid type adder the performance was improved. The modified booth encoder will reduce the number of partial products generated by a factor of 2. Fast multipliers are essential parts of digital signal processing systems. The speed of multiply operation is of great importance in digital signal processing as well as in the general purpose processors. The number to be added is the multiplicand, the number of times that it is added is the multiplier, and the result is the product. Each step of addition generates a partial product. the simulation is done on the Modelsim and finally output is displayed on Matlab.

Keywords: - VLSI, Carry Select Adder(CSA), Carry Look Ahead Adder (CLA), ASM

1. Introduction to DWT

The Discrete Wavelet Transform (DWT) is the transform of choice at the heart of recent image compression algorithms. Adopted by the JPEG2000 image compression standard [1], it significantly outperforms algorithms based on other transforms, such as the discrete cosine transform, in terms of objective metrics as well as perceptual image quality [2]. The success of the DWT stems from its ease of computation and its inherent decomposition of an image into non-overlapping subbands that enables the design of efficient quantization algorithms and allows for incorporation of the human visual system. A DWT based image codec is a good choice for applications such as remote exploration, urban search and rescue operations and satellite imaging. These applications require transmission of still images from remote image acquisition devices to base stations. Images are compressed after acquisition to reduce the number of data bits that need to be transmitted back to the base station over a wired or wireless communication channel. A good hardware codec employed in these applications will have: low latency and high throughput if real-time operation is desired, low power consumption if working in an untethered, battery-driven environment, small hardware size, and most importantly, high fidelity for the reconstructed image after compression. This thesis focuses on a field programmable gate array (FPGA) implementation of a DWT codec for the biorthogonal 9/7 wavelet. This wavelet has been shown to possess properties favorable for image compression; part I of the JPEG2000 standard specifies this wavelet for lossy compression. The DWT is typically computed using a perfect reconstruction (PR) filter bank. The performance of an FPGA implementation of the filter bank depends on the following two implementation design issues:

1. the filter bank structure and filter coefficient quantization; and,
2. the hardware architecture used to implement the filter bank structure. The filter bank structure determines hardware metrics such as throughput and latency while filter coefficient quantization impacts the signal processing properties of the filter bank and determines its image compression performance. The hardware architecture of the filter bank determines properties such as latency and power consumption. This thesis investigates the first issue of filter bank implementation, namely, filter bank structure and coefficient quantization. The image compression performance of the filter bank implementation critically depends on the two perfect reconstruction (PR) conditions: the no-distortion condition and the noaliasing condition. When the irrational coefficients of the biorthogonal 9/7 wavelet filters are implemented in a floating point format, both PR conditions are satisfied and the filter bank gives perfect reconstruction under lossless compression. For fast hardware implementation on an FPGA, the filter coefficients are implemented in a multiplier less manner after representing them as sum-and-difference-of-powers-of-two (SPT). Multiplication is then achieved by shifting and adding. Thus, the filter coefficients have to be quantized, i.e. approximated by fixed point SPT representations. The number of non-zero terms in the SPT representation of a coefficient, denoted by T , provides an estimate of the hardware cost associated with implementing the coefficient. This quantization of the filter coefficients alters the no-distortion PR condition and, consequently, image compression performance is affected. the closer the quantized filter coefficients are to the un quantized coefficients, and the closer the quantized compression performance is to the un quantized performance. However, more non-zero terms means higher hardware cost. Conversely, fewer non-zero terms means lower hardware cost, but worse compression

performance. Thus there is a trade-off between hardware cost and compression performance. The filter bank structure also influences the performance of the filter bank. Cascade filter structures are more immune to coefficient quantization than direct structures and, in general result in better compression performance for the same T. Further more, polyphase structures operate at higher clock speeds than non-polyphase structures and hence result in better throughput. The lifting structure an alternative to the traditional filter bank structure offers the advantage of an orthogonal implementation that is more robust to coefficient quantization. All three structures are evaluated in terms of compression performance (using peak signal-to-noise ratio PSNR) and various hardware metrics. For each structure, optimal quantized values are found for the filter coefficients. These coefficients enable the implementation of a fast, multiplier less DWT codec that generates the best possible PSNR performance for the given structure.

2. Overview

In this thesis we used image processing using VHDL the algorithm for image compression using DWT and modified Booth algorithm for reducing the delay time for execution of the process and to reduce the storage space in hard disk.

1. Image is taken as an input using Matlab and generating the matrix of row and columns up to quantization levels [256,256] row and column.
2. The entity is generated of the input image in VHDL coding by creating 'Do file' for execution in Modelsim VHDL coding .
3. Modified Booth algorithm is applied on the input image strings rows and columns to get the partial products as output of image in VHDL coding in Modelsim.
4. Booth algorithm used as a Multiplier to generate the partial products. Application of Multiplier to enhances the speed of execution and creating a less storage space for the execution of programme.
5. The final output of Booth algorithms partial products are used as a input to DWT for image compression technic.
6. The output resultant matrix elements or Pixels of DWT is simulated on MATLAB to obtained corresponding output compressed image.

3. Draw Block diagram of your project flow chart

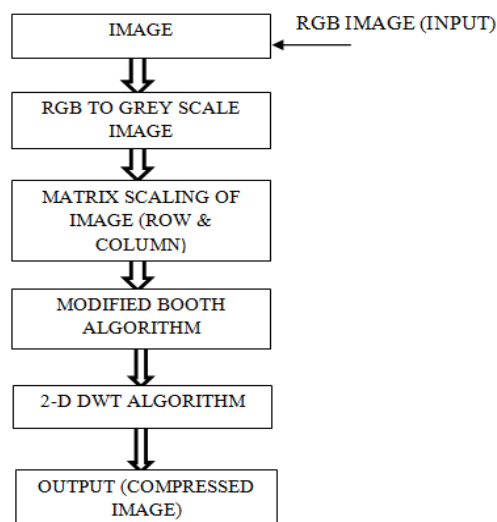


Fig. 1. Block Diagram of Project

4. Details of Block diagram

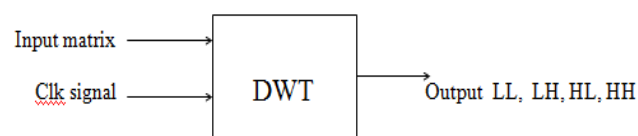


Fig 1(a). Design of Architecture of DWT

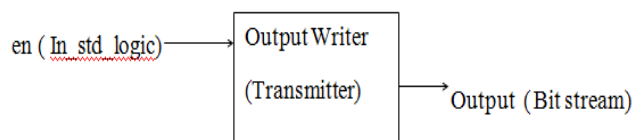


Fig 1(b). Design of Output Transmitter

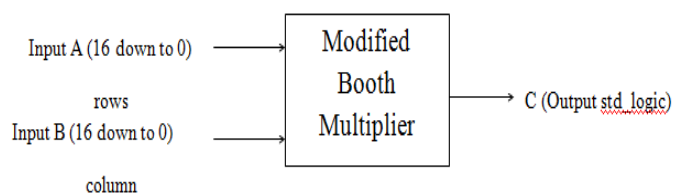


Fig 1 (c). Design of architecture of modified booth algorithm

5. Overview of DWT:

1-D DWT stands for one dimensional discrete wavelet transform. It is a transform similar to discrete fourier transform(DFT). It uses multi-resolution technique for time-

frequency analysis of signals. The main advantage of DWT compared to DFT is that we get both time and frequency analysis of a signal at the same time. The DWT is mainly used for image compression. It also has various signal processing applications. The DWT can provide significant compression ratios than the previous techniques like the Discrete Cosine Transform (DCT) and the Discrete Fourier Transform(DFT). The signal to be analyzed is passed through low pass and high pass filters. This is then followed by decimation by two. This yields the low pass sub-band_L and the high pass sub-band_H. To reconstruct the original signal we first do interpolation followed by low pass and high pass filtering. This is illustrated in the figure below.

5.1 Wavelets Multi-resolution analysis:

- Example: consider the sequence of pixels: 10 8 1 3 5 7 8 6
- averages: [9 2 6 7] differences: [-2 2 2 -2]
- averages: [5.5 6.5] differences: [-7 1]
- averages:[6] differences: [1]
- Each stage divides the band into 2 subbands - low frequency + high frequency coefficients
- Regions of discontinuities will have large coefficients, smooth regions will have smaller differences
- Error introduced by truncating a coefficient is proportional to its magnitude, can truncate small coefficients without considerable distortion

5.2. 1-D DWT for Image Compression:

- DWT coefficients of input image - multiple levels of wave-letting
- Coefficients are quantized - coefficients in each subband is quantized separately
- Coefficients are zero thresholded, different subbands have different thresholds
- Longs spells of zero are run length encoded
- The coefficients are then entropy encoded

5.3 DWT Algorithm:

A)Design Specification

- Input image: 512x512 pixel, gray scale frame, 8 bits/pixel
- Support 3 different configurations of encoder with varying levels of compression

B)Design Partition - 2 stages

- Stage 1: DWT coefficients over 3 stages of wave-letting
- Stage 2: Dynamic Quantization, Zero thresholding, RLE of zeroes and, Entropy encoding of DWT coefficients
- 2 stages are implemented on 2 separate PEs

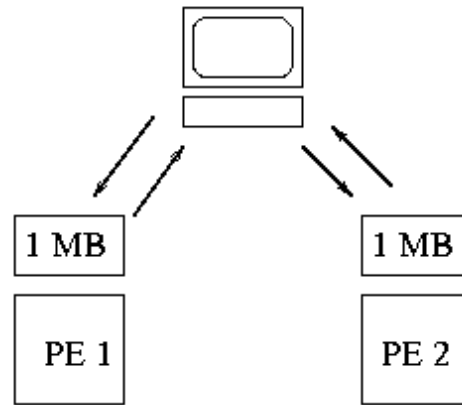


Fig 2. Stages of implementation

Stage 1 - DWT coefficients

- **Input:** 8 bit pixels, **Output:** DWT coefficients - 16 bits
- 2 pixels/WORD, 512 Rows and 256 Columns, 0.5 MB
- From 512 pixels in a row, extract 256 low frequency coefficients + 256 high frequency coefficients
- Symmetric extension at the boundaries

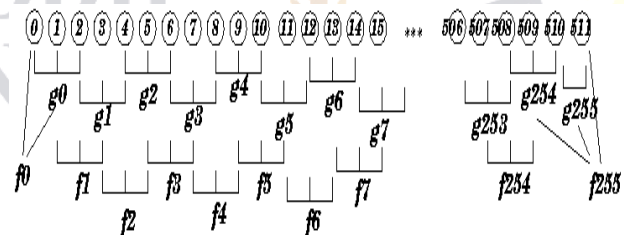


Fig 2 (a). Symmetric Extention and boundaries

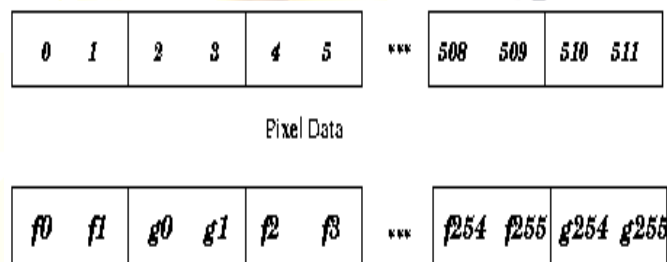


Fig 2(b). Design Partition on stage 1 of length 512

Stage 1 - DWT coefficients

- Extend same scheme of interleaved memory access along Y direction
- But now the 2 values obtained in a READ are not consecutive pixel values of a column rather they are one pixel each of two parallel columns
- 3 stages of Wave-letting
- Stage 1 - On rows and columns of length 512
- Stage 2 - On rows and columns of length 256
- Stage 3 - On rows and columns of length 128

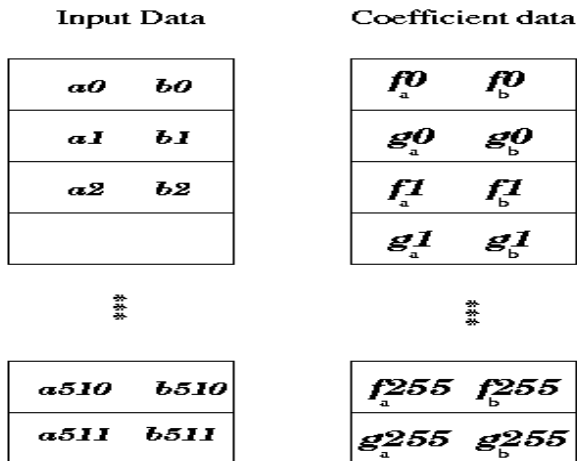


Fig 2(c). Design Partition on stage 2 of length 256

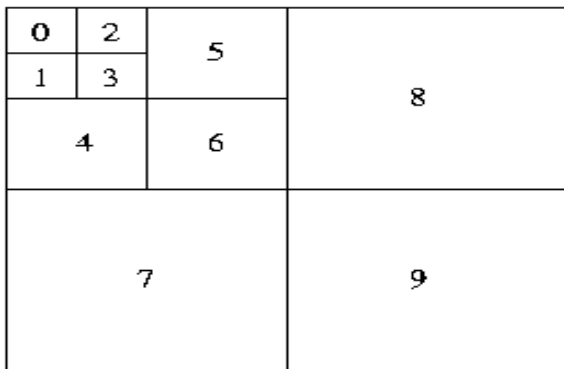


Fig 2 (d). Design Partition on stage 3 of length 128

6. Why adaptive image compression?

Image processing systems can encode raw images with different degrees of precision, achieving varying levels of compression. Encoding can be achieved with different encoders with varying compression ratios. The need to dynamically adjust the compression ratio of the encoder arises in many situations. One example involves the real-time transmission of encoded data over a packet switched network. On detecting network congestion, the encoder can cut down the precision and gain more compression, rather than waiting for some packets to be dropped. To suitably adapt the encoder to the varying compression requirements, adaptive adjustments of the compression parameters are required. This involves reconfiguring the encoder in some sense.

7. Radix-4 Booth Multiplier

With the help of recent advances in multimedia and communication systems, real-time signal processing like audio signal processing, video/image processing, or large capacity data processing are increasingly being demanded. The multiplier and multiplier-and-accumulator (MAC) are the essential elements of the digital signal

processing such as filtering, convolution, and inner products. Most digital signal processing methods use nonlinear functions such as discrete cosine transform (DCT) or discrete wavelet transform (DWT), because they are basically accomplished by repetitive application of multiplication and addition. Booth recoding is a technique for high speed multiplication, by recoding the bits that are multiplied. The number of partial products reduced to half, using the technique of radix-4 Booth recoding [1],[2][6].

7.1 Algorithm:

Modified Radix-4 Booth's Algorithm is made use of for fast multiplication. The salient features of this algorithm are:

- Only $n/2$ clock cycles are needed for n -bit multiplication as compared to n clock cycles in Booth's algorithm.
- Isolated 0/1 are handled efficiently.
- For even n , the two's complement multipliers are handled automatically whereas for odd n an extension of sign bit is required. Procedure: For all odd values of i where i ranges from 1 to $n-1$ for n -bit multiplication (assuming n is even), the bits of the multiplicand are recoded using the formula

$$y_i = x_{i-1} + x_{i-2} - 2x_i$$

Then multiplication is done in normal way with the y_i that have been calculated. The following example illustrated the whole procedure

A		01	00	01	17
X	x	11	01	11	-9
Y		$0\bar{1}$	10	$0\bar{1}$	recoded multiplier operation
Add $-A$	+	10	11	11	
2-bit Shift		1	11	10	11
Add $2A$	+	0	10	00	10
		01	11	01	11
2-bit Shift		00	01	11	01
Add $-A$	+	10	11	11	
		11	01	10	01
					-153

Fig 3. Modified Radix-4 booth Multiplication

8. Radix-4 Modified Booth Multiplier Algorithm

The modified Booth algorithm minimises the number of partial products by half. We used the modified Booth encoding (MBE) scheme. It is known as the most efficient Booth encoding and decoding scheme. To multiply, multiplicand 'X' by multiplier 'Y' using the modified Booth algorithm. First group the multiplier bits 'Y' by three bits and encoding into one of {-2, -1, 0, 1, 2}. Prior to convert the multiplier, a zero is appended into the Least Significant Bit (LSB) of the multiplier. Table I shows the rules to generate the encoded signals by MBE scheme and Fig. 2 (a) shows the corresponding logic diagram. The Booth decoder generates the partial products using the encoded signals [1][7].

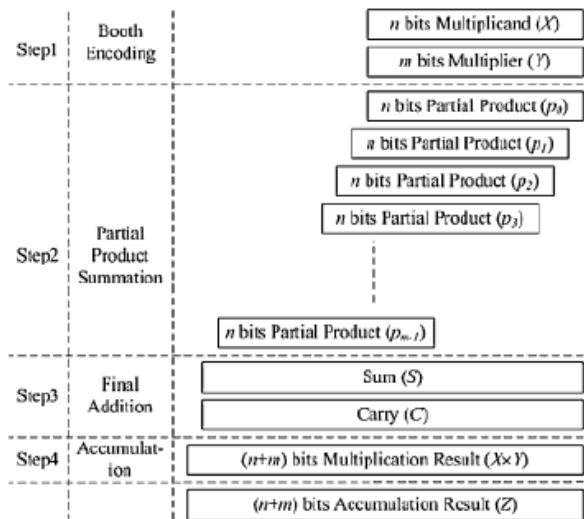


Fig 4. Basic arithmetic steps of multiplication and accumulation[1],[2][8].

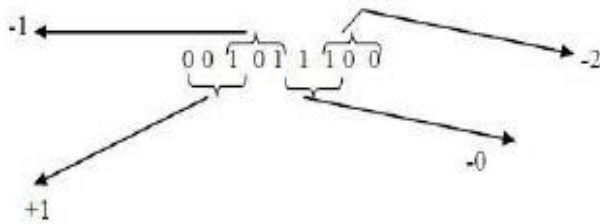


Fig 5. Booth Recoding [2][9].

Table 1 : Radix 4 Booth Table

Select Line (Encoding)	Partial Products (Operation)
000	Add 0
001	Add multiplicand
010	Add multiplicand
011	Add 2* multiplicand
100	Subtract 2* multiplicand
101	Subtract multiplicand
110	Subtract multiplicand
111	Subtract 0

The recoding is done by appending one zero to the Least Significant Bit (LSB) and extending the Most Significant Bit (MSB) with the sign bit if necessary. Then the grouping of 3 bits from the LSB is done as shown in Fig 2. The obtained result is -1 -1 0 -2. This result is multiplied with the multiplier and the number of partial product is reduced [2][11].

9. VLSI Architecture Implementation

The architecture of the proposed ECAT Booth multiplier is designed by using tree-based carry save reduction followed by parallel-prefix carry-propagate addition architecture. The whole architecture of the proposed ECAT Booth multiplier is shown in Fig.accumulator. In final adder both sum and carry is added to produce the 2N bits product.

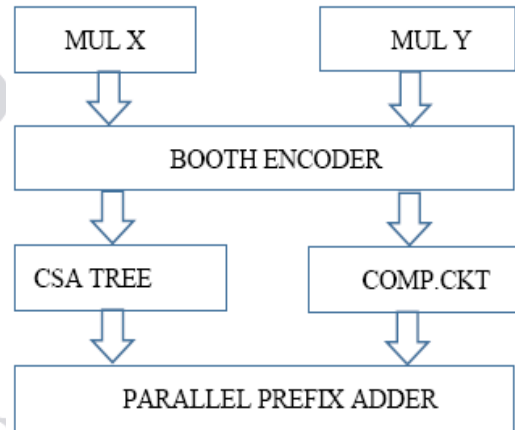


Fig 6. VLSI Architecture [2][12].

10. Architecture of A Multiplier

- A multiplier can be divided into three operational steps:
- Radix-4 Booth algorithm in which a partial product is generated.
 - Carry save adder and Accumulator
 - The final addition in which the final multiplication result is produced by adding the sum and the carry

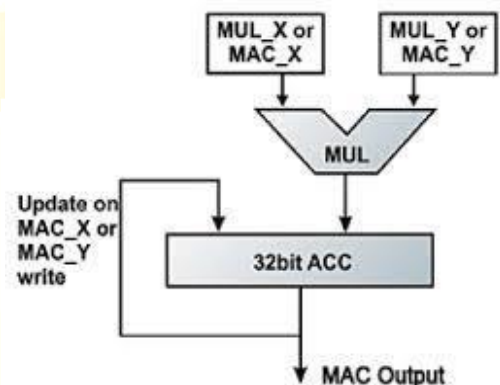


Fig 7. MAC Multiplier[1][11].

Generally if N-bit data of multiplicand 'X' is multiplied with N-bit multiplier 'Y' then it generates N- partial products. But if Radix-4 booth algorithm is used then number of partial products will be reduced to N/2. In addition, the signed multiplication based on 2's complement numbers is also possible.

$$X = -2^{N-1}x_{N-1} + \sum_{i=0}^{N-1} x_i 2^i, \quad x_i \in 0, 1$$

$$X \times Y = \sum_{i=0}^{\frac{N}{2}-1} d_i 2^{2i} Y$$

Where $d_i = -2x_{2i+1} + x_{2i} + x_{2i-1}$

$$P = X \times Z = \sum_{i=0}^{N/2-1} d_i 2^i + \sum_{j=0}^{2N-1} 2^j$$

In CSA, the sign extension is used in order to increase the bit density of the operands. Half adder is used to generate sum and carry in CSA. The generated carry is stored in accumulator [1][11].

11. 2-D Discrete Wavelet Transform

The main challenges in the hardware architectures for 1-D DWT are the processing speed and the number of multipliers and adders while for 2-D DWT it is the memory issue that dominates the hardware cost and the architectural complexity. A 2-D DWT is a separable transform where 1-D wavelet transform is taken along the rows and then a 1-D wavelet transform along the columns. The 2-D DWT operates by inserting array transposition between the two 1-D DWT. The rows of the array are processed first with only one level of decomposition. This essentially divides the array into two vertical halves, with the first half storing the average coefficients, while the second vertical half stores the detail coefficients. This process is repeated again with the columns, resulting in four sub-bands within the array defined by filter output as in three-level decomposition.

The LL sub-band represents an approximation of the original image, the LL1 sub-band can be considered as a 2:1 sub-sampled version of the original image. The other three sub-bands HL1, LH1, and HH1 contain higher frequency detail information. This process is repeated for as many levels of decomposition as desired. The JPEG2000 standard specifies five levels of decomposition, although three are usually considered acceptable in hardware. In order to extend the 1-D filter to compute 2-D DWT in JPEG2000, two points have to be taken into account. Firstly, the 1-D DWT generates the control signal memory to compute 2-D DWT and manage the internal memory access. Secondly, we need to store temporary results generated by 2-D column filter. The amount of the external memory access and the area occupied by the embedded internal buffer are considered the most critical issues for the implementation of 2D-DWT. As the cache is used to reduce the main memory access in the general processor architectures, in similar way, the internal buffer is used to reduce the external memory access for 2D-DWT. However, the internal buffer would occupy much area and power consumption. Three main architecture design approaches were proposed in the literature with the aim to implement efficiently the 2D-DWT level by level, line-based

and block based architectures. These architectures address this difficulty in different ways. A typical level-by-level architecture as uses a single processing module that first processes the rows, and then the columns. Intermediate values between row and column processing are stored in memory. Since this memory must be large enough to keep wavelet coefficients for the entire image, external memory is usually used. Access to the external memory is sometimes done in row-wise order, and sometimes in column-wise order, so high-bandwidth access modes cannot be used. 157 external memory access can become the performance bottleneck of the system for the given J level of decomposition [3][12][14].

12.1 Image Acquisition:

Electronic devices such as optical (digital/video) camera, webcam etc can be used to capture the acquired images. In our project we have taken sample picture images. As shown in figure below



Fig 8. Input JPEG Image taken from gallery.

12.2 RGB Image to Gray scale image:

In photography and computing, a gray scale digital image is a picture within which the worth of every constituent may be a single sample, that's it carries solely intensity data. Pictures of this kind, additionally celebrated as black-and-white, are composed exclusively of reminder gray, varying from black at the weakest intensity to white at the strongest. In grey scale pictures, however, we have a tendency to do not completely differentiate however abundant we have a tendency to emit of the different colors we have a tendency to emit the same quantity in every channel. What we will differentiate is that the total quantity of emitted lightweight for every pixel; very little lightweight offers dark pixels and far lightweight is perceived as bright pixels. When converting an RGB image to gray scale, we've to require the RGB worth's for every constituent and build as output one value reflective the brightness of that constituent. One such approach is to require the typical of the contribution from each channel: $(R+B+C)/3$. The red, in experienced and Blue parts square measure separated from the twenty four bit color worth of every constituent (i,j) to calculate the eight bit grey worth victimization the formula. The Fig. below shows the gray scale image.

12.3 Insert black & white Image of Matlab



Fig 9. Output JPEG Image after simulation.

13. CONCLUSION

In this paper, we have analyzed the 2-D Discrete Wavelet Transform by using Radix 4-booth multiplier and computational time for the different architectures. This result is useful for converting the RGB image into grey scale image and exploring a new method pipelined of handling multiple data streams suitable for application in image and video processing multimedia real time applications. When down sampling in wavelet transform we need to multiply the row and column with the down sampling factor, this multiplication is being done by the booth multiplier. that is why we are getting better output as compared to Normal Multiplication. Hence the time by normal booth Multiplier is 521225010 ns and time taken by Radix-4 Booth multiplier is 26061000 ns hence near about 50% power reduction than the conventional Normal Booth Multiplier.

14. Simulation Result & Analysis

14.1. Simulation Result:

14.1(a) Input selection of an image:

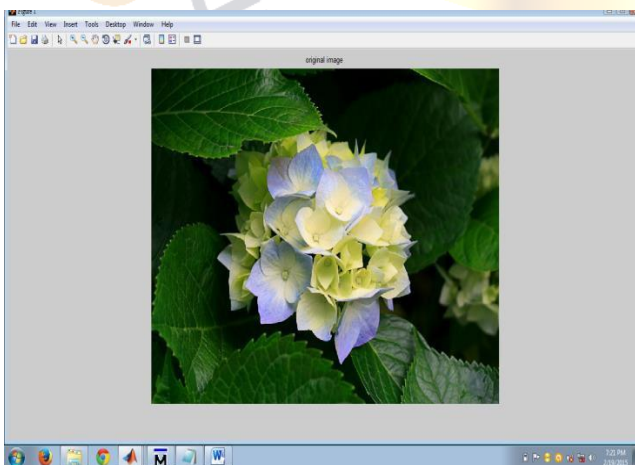


Fig 10.1 Input Image

14.1 (b) RGB to Gray Scale Image:

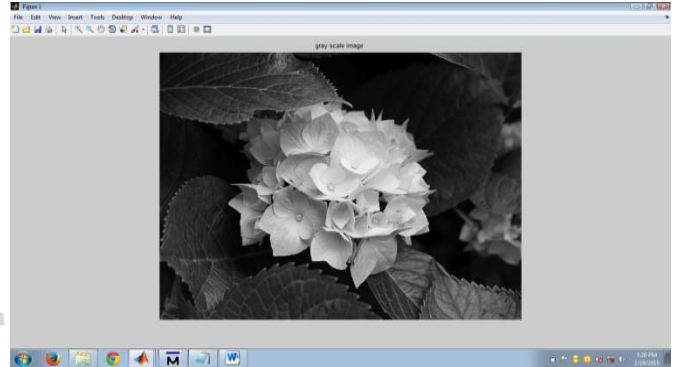


Fig 10.2 Output Image

14.2 (c) Simulation on VHDL coding on Model Sim 6.3F of MBA_DWT algorithm :

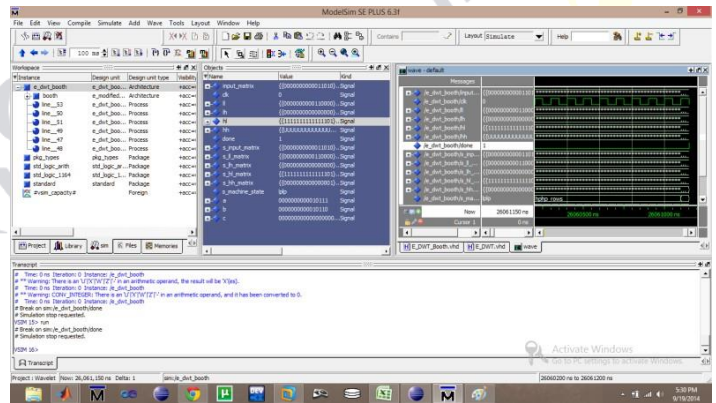


Fig 10.3 Simulation on Modelsim

14.3 (d) Output Writer :

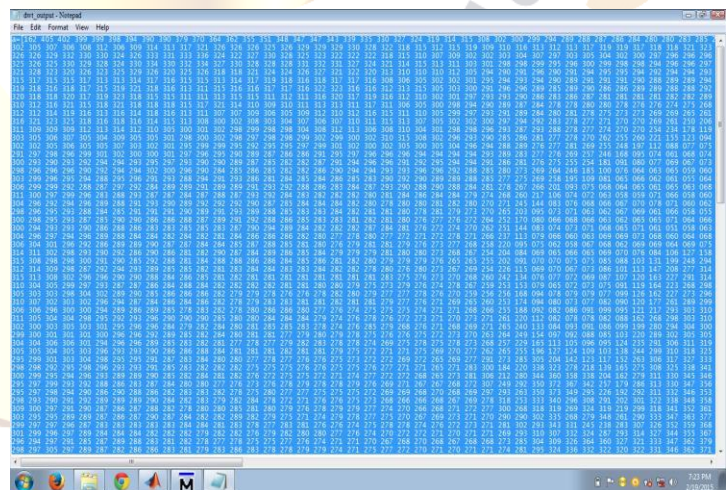


Fig 10.4 DWT_output

14.4 (e) Output Result of Simulation using Matlab:

15. REFERENCES

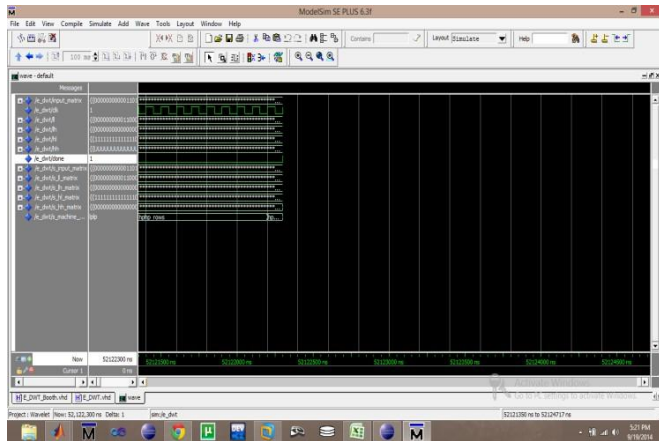


Fig 10.5 Simulation Result.

14.5 (f) Final Output after simulation.

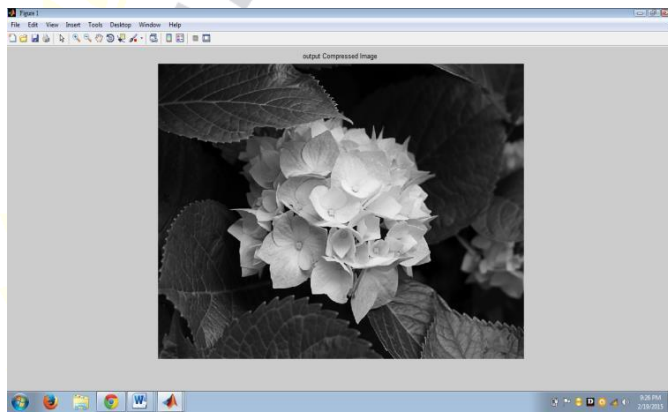


Fig 10.6 Final output figure.

14.5 (g). Output waveform in Test Bench Waveform

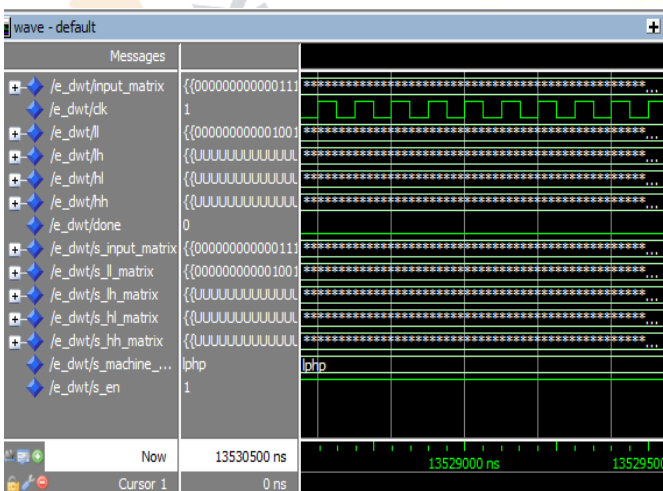


Fig 10.7 Test Bench waveform

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