Improvement Strategies for Multilevel Inverters Using PWM

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Abstract — It was determined that PD-SPWM produced the highest CMV amplitude of one-third the dc bus voltage, but the lowest values of differential-mode dv/dt, THD, and drive losses. The second strategy, phase-opposition (PO)-SPWM, reduced the CMV amplitude to one-sixth the dc bus voltage, at the cost of higher THD and drive losses and a doubling of the differential-mode dv/dt. The final strategy, zero common-mode (ZCM)-SPWM, was modified (MZCM-SPWM) to accommodate IGBT dead-time by delaying the output voltage transitions based on the polarity of the output currents and the direction of the commanded voltage transitions. The MZCM-SPWM method nearly eliminated all CMV pulses while maintaining comparable levels of THD, but produced twice the switching losses compared to PD- and PO- SPWM, and twice the differential-mode dv/dt compared to PD-SPWM.

Keywords — Total Harmonic Distortion (THD), CMV, MATLAB, SPWM.

1. INTRODUCTION

The research and growth of multilevel voltage-source power electronic energy conversion equipment has been profound over the last several decades, owed mainly to the decreasing cost and increasing reliability of high power semiconductor devices. These power converters are popular in medium and high voltage applications due to their ability to handle high voltages without compromising the output power [1, 2], thus eliminating the need for transformers to increase or decrease voltage levels [3], which pose considerable size, weight, and cost penalties. Multilevel converters (MLCs), in inverter or rectifier mode, are also emerging in low voltage applications because of their ability to produce low levels of total harmonic distortion (THD) in the output voltage and current compared to conventional two-level converters [1].

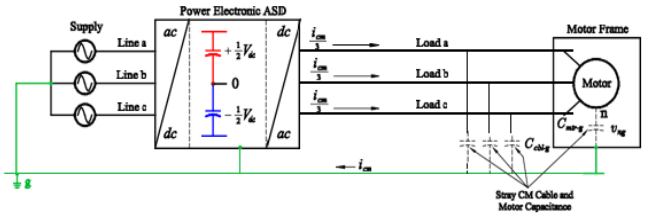
2. Common Mode Voltage and its Effects in AC Motor Drive Systems

In any balanced ac three phase motor system with purely sinusoidal excitation, the phase voltages with respect to the neutral point of the motor (assuming a Y connection) are composed of only positive sequence components, thus the instantaneous sum of the time-domain phase voltages is zero [10]. This situation is normally applicable to motors that are connected directly to the utility mains. The major drawback of this scenario is the inability to control the motor speed and torque, resulting in less than optimal control and operating efficiency. Furthermore, the inrush currents when direct-line starting is employed can reach levels exceeding six times the rated current of the motor [11].

FIGURE 1: SOURCE-DRIVE-MOTOR SIMPLIFIED CIRCUIT SHOWING CABLE AND MOTOR PARASITIC CAPACITANCES AND CMI PATHS.

3. CMV and CMI Mitigation Strategies

There have been numerous studies on the mitigation of CMV and CMI produced by VSI ASDs for both two



level and multilevel topologies. Hardware solutions have been proposed that add additional components to the ASD, the load, or both. There are penalties with this option due to the additional size, weight, and cost of the components. The other option is to modify the PWM algorithm to reduce the amplitude of the CMV and its number of occurrences over each switching period.

3.1 Hardware *Solutions to Reduce CMV/CMI/EMI*

Adding electrical hardware to the ASD system is one of the primary solutions for reducing the levels of CMV and CM *dv/dt*., and several existing strategies will be presented in this section. An early and popular approach in industry is the use of shaft grounding brushes [19, 26], which shunt the common mode current induced by the shaft voltage to ground by providing a low impedance connection directly to the motor shaft. These devices require additional cost and maintenance and may not be suitable is harsh or explosive environments.

3.2 *Software Solutions to Reduce CMV Amplitude*

The other option to reduce CMV and CM dv/dt is through the modification of the PWM algorithm internal to the ML-ASD controller. This section will focus on existing CMV mitigation PWM algorithms in literature related to the NPC VSI, mainly the three-level NPC VSI for the sake of clarity.

There are three primary criteria to consider for mitigating the harmful effects of CMV and CMI for which the PWM strategy can control:

1. The magnitude of the CMV.
2. The step height of a CMV pulse.
3. The number of CMV transitions occurring over a cycle.

4. Existing Two-Level Topologies

The two-level VSI still remains extremely popular in LV applications, especially when used as ASDs. Figure 2 represents the general circuit topology of the three phase, two-level VSI. There are a total of six active switches, each equipped with an anti parallel freewheeling diode. Each phase of the load is connected to the midpoint of an inverter "leg" or "pole," which can take on two different states with respect to the dc bus midpoint, $+{}^{1}/_{2}V_{dc}$ if $Sx1$ is energized or $-{}^{1}/_{2}V_{dc}$ if $Sx2$ is energized, where $x = \{a,b,c\}$.

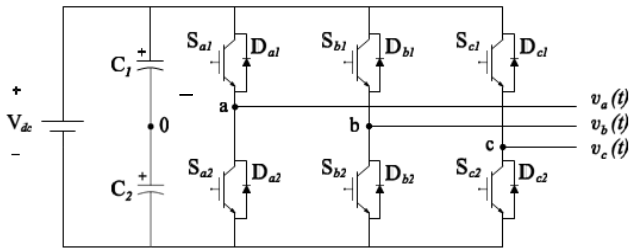


Figure 2: General topology of a two-level VSI.

4.1 Multilevel Inverters (ML-VSIs)

An ML-VSI is any inverter that produces three or more levels in the output pole voltage. This is accomplished by adding additional semiconductor switches, dc power supplies, capacitors and/or diodes. There are three main classifications of ML-VSIs, and each will be discussed in this section. The categories include:

(1) diode-clamped or NPC MLIs,
(2) flying capacitor (FC) or capacitor clamped MLIs,
(3) cascaded H-bridge (CH) MLIs.

4.2 *Neutral Point Clamped Multilevel Inverter (NPC MLI)*

The three-level PWM controlled NPC MLI , and its topology is shown in Figure 3. Five years later, Carpita and Tenconi extended the three-level NPC MLI to *m* levels. The major features and operating principles of an *m* level NPC MLI can be described. Like the two level VSI, each output phase of the ML NPC VSI is connected to the midpoint of the switches in each inverter pole.
Again, each switch is fitted with a freewheeling diode, and each phase requires the addition of clamping diodes.

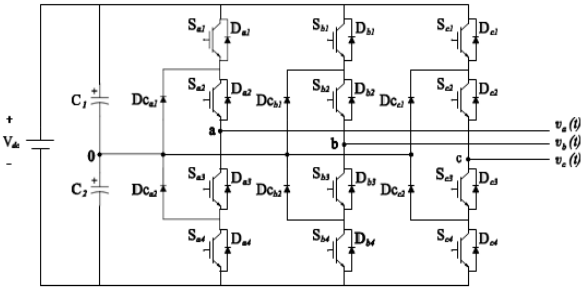


Figure 3: Topology of a three-level NPC ML-VSI.

4.3 *Flying Capacitor Multilevel Inverter (FC MLI)*

The FC MLI exhibits many of the same characteristics as the NPC MLI, such as the dc bus and active switch arrangement, output voltage, and CMV levels. The FC MLI was first proposed in 1996 by Meynard and Foch, and its three-level topology. The major difference between the FC MLI and NPC MLI is that a capacitor is substituted for the two clamping diodes in each inverter pole, which are left floating with respect to the midpoint of the dc bus.

5. PWM for Three-Level Inverters

Controlling a three-level VSI with PWM is the most popular technique used in motor-drive systems because it offers significant advantages over the traditional commutation methods. In order to reduce the losses and torque pulsations, harmonic content in the output must be minimized. To achieve this, three-level PWM schemes have been developed and incorporated into three- level ASDs rather than operating in the conventional 12-step commutation mode, which has poor harmonic performance owed to the square-wave output voltages.

5.1 Topology and Operation of the Three-level NPC ASD

The three-level NPC ASD to be investigated and analyzed in this paper. Each inverter pole consists of four series-connected IGBTs $Sx1$, $Sx2$, $Sx3$, $Sx4$,

$x = \{x = a,b,c\}$ with their associated antiparallel diodes and connected across the dc bus and two clamping diodes Dc $x1$, Dc x 2 with their common point connected to the midpoint of the dc bus.

5.2 Carrier-based Sub-Harmonic PWM

The key objective of any SPWM algorithm is to discretely control switching commutations by comparing a commanded reference waveform to a higher frequency carrier waveform to produce output voltages that replicate the reference signal with the highest degree of accuracy. There are a wide range of ML SPWM categories, depending on the characteristics of the reference waveform, the carrier waveforms, or both.

5.3 In-Phase Disposition Sub-harmonic PWM (PD-SPWM)

This method is the first of three SPWM techniques that will be investigated in this thesis. Because it is a classic three-level PWM method, it will be used to further elaborate on SPWM theory of operation and address the issues of ZSI, DT, and midpoint balancing problems.

6. SIMULATION AND RESULTS

The three SPWM methods (PD- SPWM, PO-SPWM, and MZCM-SPWM) were modeled in a simulation environment using two software programs. The PLECS blockset software program was utilized to acquire steady-state time- and frequency-domain waveforms of the output currents, output voltages, and CMV operating at a PWM factor of 0.628, which corresponds to a dc bus utilization of approximately 70%. The PLECS program was also used for a sweep of the PWM factor to acquire spectral and thermal data for the analysis of harmonic distortion, inverter losses, and efficiency.

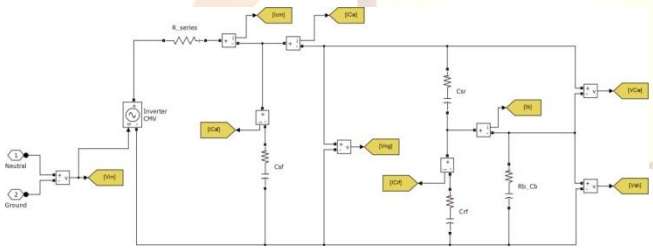


Figure 4: Simulink equivalent CM circuit for shaft voltage/bearing current analysis.

The simulated output currents in Figure 5 are nearly sinusoidal and highly symmetrical, with negligible harmonic content greater than the fundamental, as illustrated in the FFT of the simulated phase *a* current shown in Figure 6, which supports the effectiveness of using three-level NPC VSIs.

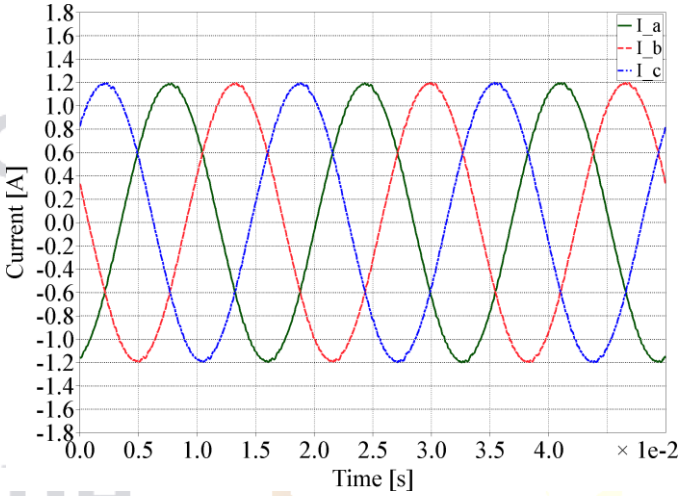


Figure 5: Simulated time-domain waveforms of output line currents using PD- SPWM.

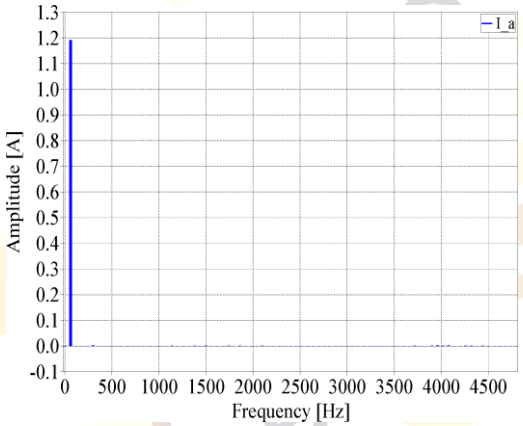


Figure 6: FFT of simulated phase *a* output current using PD-SPWM

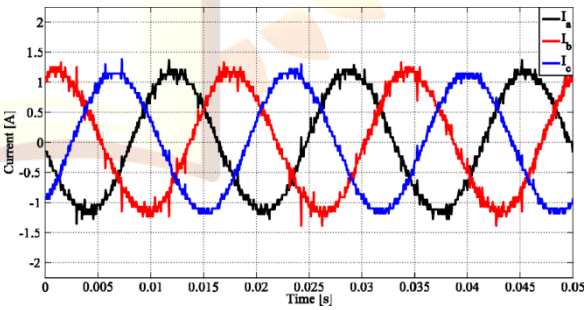


Figure 7: Measured time-domain waveforms of output line currents using PD- SPWM.

On the contrary, there is substantial noise associated with the measured currents shown in Figure 7. The noise may be a result of high frequency coupling, see the spectrum in Figure 8, between the output conductors (which are unshielded between the ASD output and the motor) and the nearby dc bus conductors. The LC output filter may have substantially reduced this noise, however it was not used for the experimental analysis for the purposes of verifying the CMV produced by the NPC ASD.

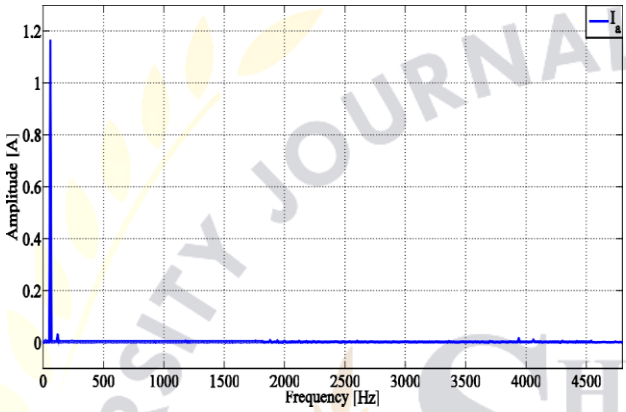


Figure 8: FFT of measured phase *a* output current using PD-SPWM.

The PO-SPWM algorithm, which involves the phase shifting of one of the two triangular carrier waves by 180 degrees compared to PD-SPWM, produces a profound decrease in the CMV amplitude. As illustrated in Figure 9, the *vn* 0 CMV produces voltages of ± 16 V_{dc} and 0 V_{dc}, which validates the use of only 19 of the 27 three-level switching states. Hence, the six small redundant vectors that produce a CMV of ± 13 V_{dc} are completely avoided when using the PO-SPWM technique, which simulation results showed to be valid over the entire tested range of PWM factor.

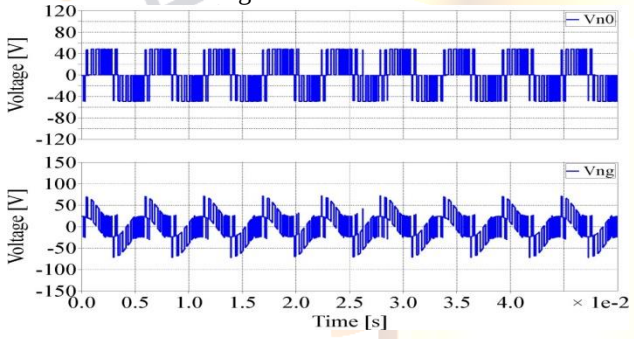


Figure 9: Time-domain waveforms of load neutral to dc bus midpoint CMV (top) and load neutral to frame ground CMV (bottom) using PO-SPWM.

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