Hardware Efficient Design of FLASH ADC Encoder for Binary Codes

Puja Kumari[1], Sachin Bandewar[3]
[1]Research Scholar [2]Assistant Professor
[1,2] Department of ECE, Sri Satya Sai College of Engineering, RKDF University, Bhopal, M.P
[1]pujasaruktr@gmail.com, [2]sachin.bandewar9@gmail.com

ABSTRACT

The performance of Flash Analog-to-Digital converter is greatly influenced by the choice of Comparator and Thermometer-to- Binary encoder design. The work describes the design and pre-simulation of a , 3bit and an 4bit analog to digital converter for low power CMOS. It requires 2^N-1 comparators, an encoder to convert thermometer code to binary code. The design is simulated in cadence environment using spectre simulator under 90nm technology. The pre simulation results for the design shows a low power dissipation of 87uw for the comparator and 1.05mW and 1.984mW power dissipation for 3-bit and 4-bit Flash ADC respectively. The circuit operates with an input frequency of 25MHz and 1.5V supply with a conversion time of 2.162ns and 6.182ns for 3-bit and 4-bit ADC respectively.

Keywords

Low-power, CMOS comparator, Flash ADC, Thermometer encoder.

1. INTRODUCTION

An **analog-to-digital converter** (ADC) is a device that converts the input continuous physical quantity to a digital number that represents the quantity's amplitude. The result is a sequence of digital values that have converted a continuous- time and continuous-amplitude analog signal to a discrete- time and discrete-amplitude digital signal. A direct- conversion ADC or flash ADC has a bank of comparators sampling the input signal in parallel, each firing for their decoded voltage range. The comparator

2. FLASH CONVERTER

Flash ADCs (sometimes called parallel ADCs) are the fastest type of ADC and use large numbers of comparators. The input signal is applied to all the comparators at once, so the thermometer output is delayed by only one comparator delay from the input, and the encoder N-bit output by only a few gate delays on top of flash ADC consists of 2^N resistors and 2^N–1 comparators arranged as in Figure Fig 1. Each comparator has a reference voltage which is 1 LSB higher than that of the one below it in the chain. For a given input voltage, all the comparators below a certain point will have their reference voltage and a “1” logic output, and all the comparators above that point will have a reference voltage larger than the input voltage and a “0” logic output. The 2^N–1 comparator outputs therefore behave in a way analogous to a mercury thermometer, and the output code at this point is sometimes called a thermometer code. Since 2^N–1 data outputs are not really practical, they are processed by a decoder to generate an N-bit binary output.

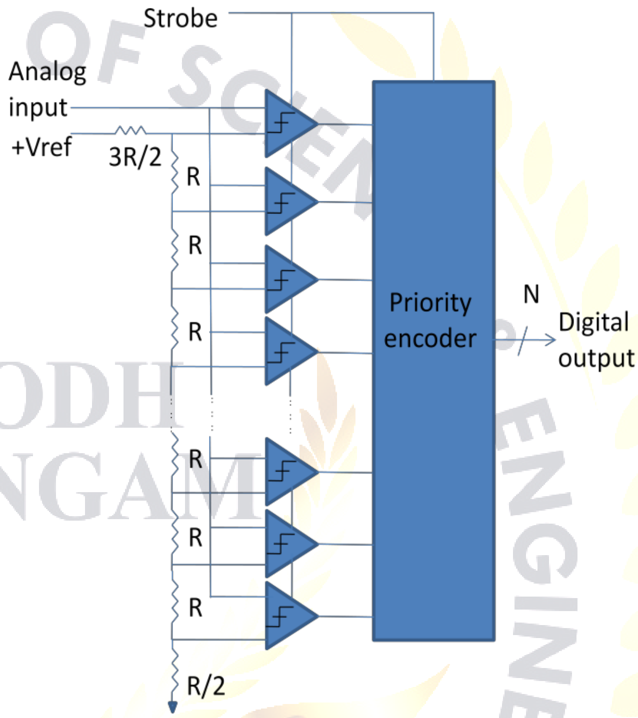

Figure 1: N-Bit Flash

The architecture uses large numbers of and comparators and is limited to low resolutions, and if it is to be fast, each comparator must run at relatively high power levels. Hence, the problems of flash ADCs include limited resolution, high power dissipation because of the speed comparators and relatively large (and therefore expensive) chip sizes. In addition, the resistance of the reference resistor chain must be kept low to supply adequate bias current to the fast comparators.

2.1 Comparator

The low power comparator circuit used in the design of Flash ADC is shown in fig 2 which is proposed in [1]. This circuit uses a preamplifier and a latch stage. In the preamplifier stage to achieve an acceptable gain the input differential pair uses NMOS transistors and the load uses PMOS transistors. The latch stage consists of two inverters which are connected in a back to back fashion forming a differential comparator and an NMOS transistor is connected between the two differential nodes of the latch. The design was implemented in cadence using 180nm technology [1]. In our proposed work pre-

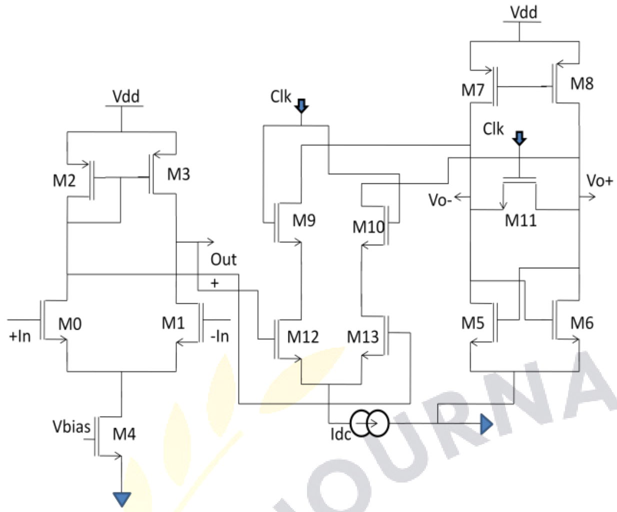

Fig 2: Preamplifier-Latch

The preamplifier stage improves the sensitivity of the comparator and isolates the comparator input from switching noise of the positive feedback stage [3]. The latch stage gives the information about which of the input signals is larger and amplifies the difference between the

2.2 Thermometer to Binary code converter

The logic encoder used for 3bit and 4bit ADC are as shown in fig 3 and fig 4. This is a multiplexer based encoder which converts thermometer codes to binary codes. Table 1 and table
2 show the truth table for 3bit and 4bit encoders. The multiplexers used are designed using transmission gates

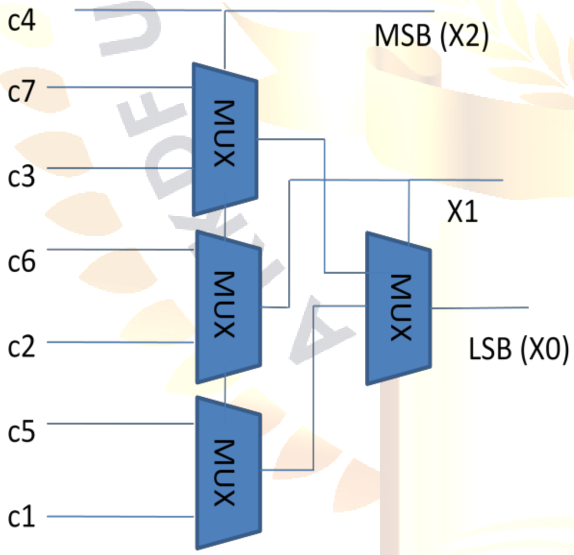

Fig 3: Logic Encoder for 3bit

Table 1: Truth table for 3bit

C7	C6	C5	C4	C3	C2	C1	X2	X1	X0
0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	0	0	1
0	0	0	0	0	1	1	0	1	0
0	0	0	0	1	1	1	0	1	1
0	0	0	1	1	1	1	1	0	0
0	0	1	1	1	1	1	1	0	1
0	1	1	1	1	1	1	1	1	0
1	1	1	1	1	1	1	1	1	0

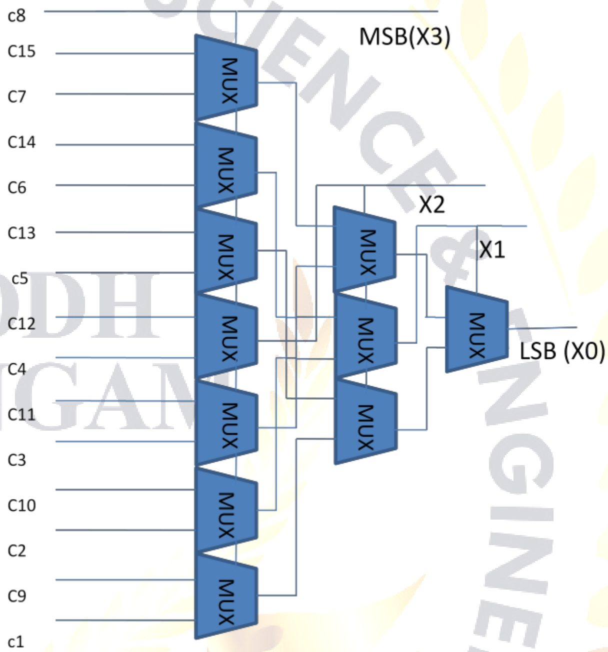

Fig 4: Logic Encoder for 4bit

Table 2: Truth table for 4bit

C15	C14	C13	C12	C11	C10	C9	C8	C7	C6	C5	C4	C3	C2	C1	X3	X2	X1	X0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1
0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0
0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	1	1
0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1	0	0
0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	1	0	1
0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	1	0
0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	1	1	1
0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0
0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	1
0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	0	1	0
0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1
0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0
0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1
0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

3. PRE SIMULATION RESULTS

3.1 Comparator output

The schematic of comparator using 90nm technology is shown in fig 4. The input signal applied to the non-inverting terminal is a sine wave and a dc reference voltage is applied to the inverting terminal of the comparator. The resulting waveform at the output of the

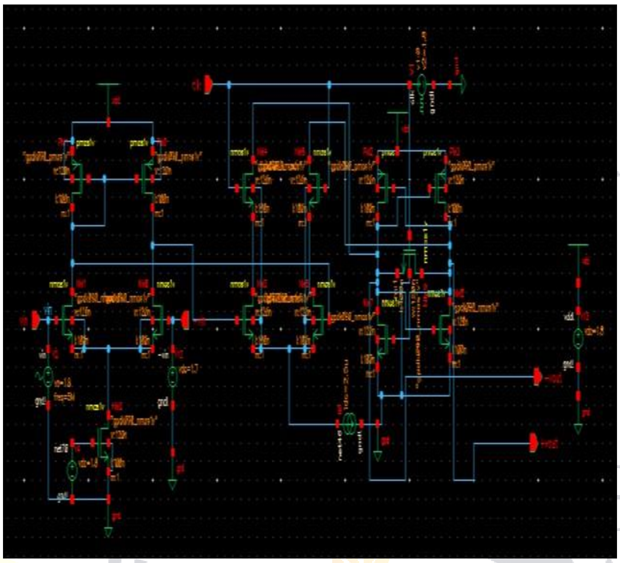

Fig 5: Schematic of

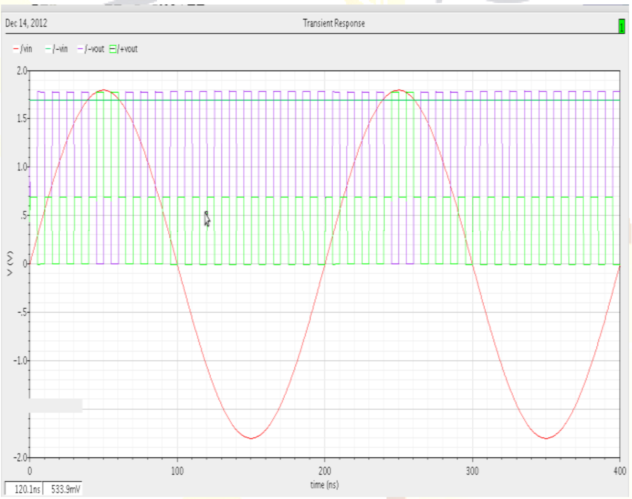

Fig 6: Comparator output

3.2 Flash ADC output

The above obtained 2^N-1 comparator outputs are encoded into 3bit output and 4bit output for 3bit and 4bit ADCs respectively using an encoder and the resulting waveform of both resolution ADCs are as shown in fig 9 and fig

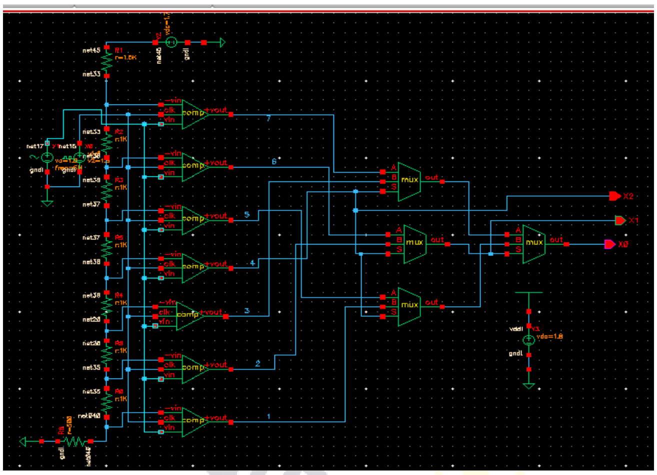

Fig 7: Schematic view of 3bit

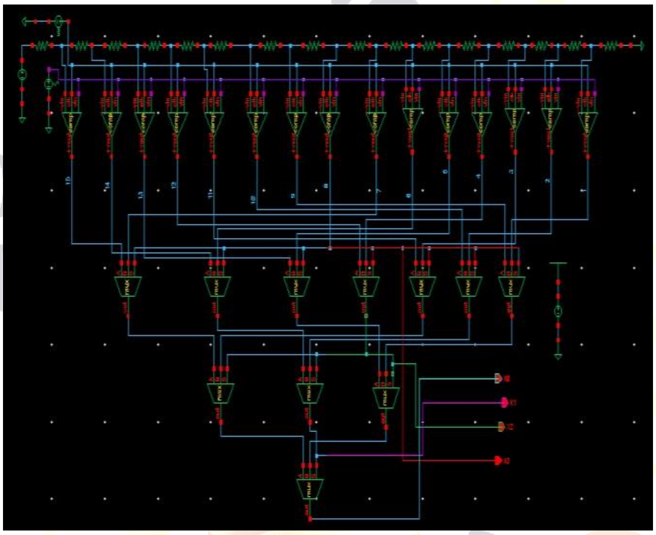

Fig 8: Schematic view of 4bit

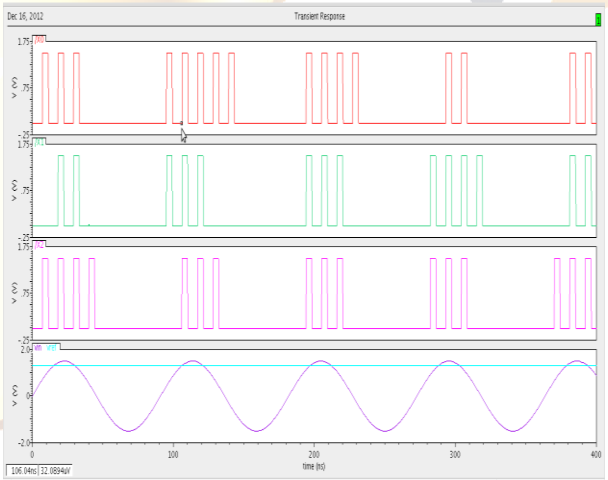

Fig 9: Output waveform of 3bit

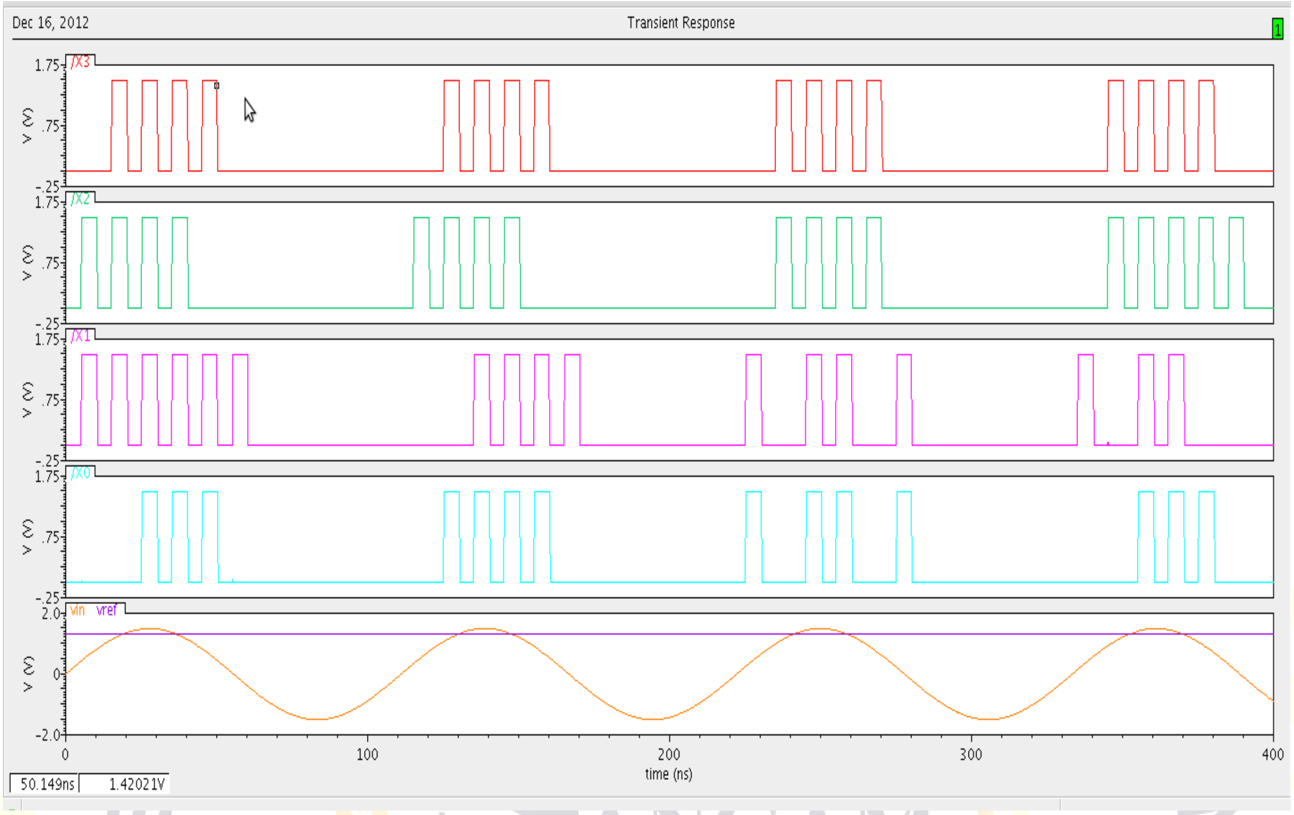

Fig 10: Output waveform of 4bit

Table 3: Comparison of Present work with earlier works for

References	Technology	Power	Voltage
[4]	350nm	200uW	2V
[5]	250nm	153uW	1.8V
[6]	180nm	132.7uW	2V
Proposed	90nm	87uW	1.5V

Table 4: Comparison of Present work with earlier works for

References	Technology	Resolution	Power	Voltage
[11]	350nm	6-bit	4.36mW	3.3V
Proposed	90nm	3-bit	1.05mW	1.5V
Proposed	90nm	4-bit	1.984mW	1.5V

Table 3 and Table 4 shows the parameter values obtained for the comparator and 4bit ADC circuit under 90nm technology with supply voltage equal to 1.5V.

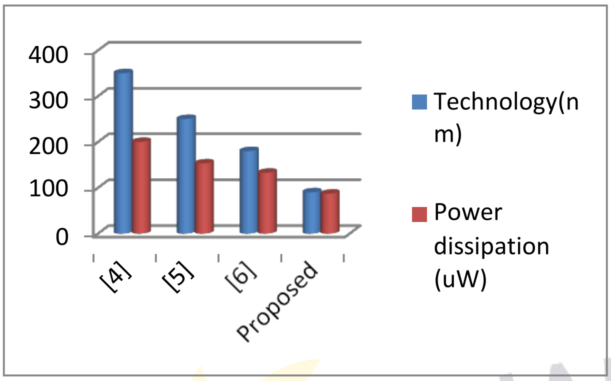

Fig 11: Comparison of Comparator results between earlier and proposed work

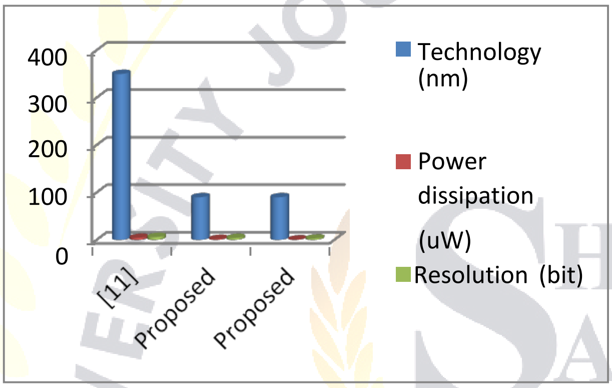

Fig 12: Comparison of ADC results between earlier and proposed work

Comparison between earlier work and proposed work for comparator and ADC results are shown in Fig 11 and

4 CONCLUSIONS

The problem of flash ADCs lies with limited resolution, high power dissipation because of the large number of high speed comparator. In this regard an attempt is made to design low- power 3bit and 4bit ADCs. The design and Pre simulation are carried out in cadence environment using spectre simulator under 90nm technology. The pre simulation results for the design shows a low power dissipation of 87uw for the comparator and 1.05mW and 1.984mW power dissipation for 3-bit and 4-bit Flash ADC respectively. The circuit operates with an input frequency of 25MHz and 1.5V supply with a conversion time of 2.162ns and 6.182ns for 3-bit and 4-bit ADC respectively. The ADC design can be used for low power and high speed applications. The proposed architecture can be extended to higher resolution. For the proposed

REFERENCES

[1] Shubhara Yewale, Radheshyam Gamad “Design of Low Power and High SpeedMOS Comparator for A/D

[2] Converter application”, Wireless Engineering and Technology, 2012, 3, 90-95.

[3] B. Razavi, “Deign of Analog CMOS Integrated Circuits,” Tata McGraw-Hill, Delhi, 2002.

[4] R. Wang, K. Li, J. Zhang and B. Nie, “A High IEEE International Workshop on Anti-counterfeiting, Se- curity, Identification, Xiamen, 16-18 April 2007, pp. 28- 31.

[5] Y. Degerli, N. Fourches, M. Rouger and P. Lut, “Low Power Autozeroed High-Speed Comparator for the Read- out Chain of a CMOS Monolithic Active Pixel Sensor Based Vertex Detector,” IEEE Transactions on Nuclear Science, Vol. 50, No. 5,

[6] 2003, pp. 1-21.

Y. Sun, Y. S. Wang and F. C. Lai, “Low Power High Speed Switched Current Comparator,” IEEE 14th Inter- national Conference, Ciechocinek, 21-23

[7] June 2007, pp. 305-308.

M. Panchore and R. S. Gamad, “Low Power and High Speed CMOS Comparator Design Using 0.18 μm Tech- nology,” International Journal of Electronic Engineering Research, Research India Publications,

[8] Vol. 2, No. 1, 2010, pp. 71-77.

W. Rong, W. Xiaobo and Y. Xiaolang, “A Dynamic CMOS Comparator with High Precision and Resolution,” IEEE Proceedings of 7th International Conference on So- lid-State and Integrated Circuits

[9] Technology, 18-21 Oc- tober 2004, pp. 1567-1570.

ShaileshRadhakrishnan, Mingzhen Wang, Chien-In Instrumentation and Measurement Technology Conference, vol. 1, pp. 287 – 292, May.

[10] Chia-Nan Yeh and Yen-Tai Lai, “A Novel Flash Analog- to-Digital Converter”, IEEE J, 2008.

[11] G. M. Yin, F. Op’tEynde, and W. Sansen, “A high-speed CMOS comparator with 8-bit resolution”, IEEE J. Solid - State Circuits, vol. 27, 1992.

[12] A.V. Bapat, Dr. A. S. Gandhi, Dr. A. M. Dighe, “CMOS Implementation of Serial Flash Analog to Digital Converter”, International Conference on VLSI, Communication & Instrumentation (ICVCI) 2011